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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,886	DENNISON, CHARLES H.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-21,23,24 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-13,15-21,23,24 and 26-29* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 9, 10 and 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9, lines 1-2, the phrase "an electrode over.....said threshold switch" is vague and indefinite. Fig. 10 discloses the upper electrode [34] is part of the threshold switch (page 10, lines 12-14). Therefore, it is believed that the upper electrode [34] is over said phase change storage element only.

Claim 15, line 2, the phrase "a periphery" is unclear whether it is being referred to the periphery of said phase change memory in claim 1.

Claim 17, lines 1-2, the phrase "etching said groove in said periphery into said sacrificial light absorbing material" is not understood. Fig. 14 discloses a portion of the insulator [44] near the groove in said periphery is being removed and a portion of the sacrificial light absorbing material near the top portion of the groove is being removed. The applicant should rewrite claim 17 so that it reflects the process step in fig. 14.

Claim 20, lines 1-3, the phrase "forming said groove in said periphery to a depth below the upper extent of said upper electrode and above the lower extent of said upper electrode" is vague and indefinite. Since claim 15 discloses the groove ([48] in fig. 12) in the periphery is formed all the way to the bottom of the phase change memory, the groove in said periphery has a depth below the upper extent of said upper electrode and below the lower extent of said upper electrode. The claim should rewrite as "forming said groove in said periphery to a depth below the upper extent of said upper electrode and below the lower extent of said upper electrode.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21 and 27 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Technische Hochschule Karl-Marx-Stadt (DD 251 225 A1 in the IDS filed on 1/21/05).

In regards to claim 21, Technische Hochschule Karl-Marx-Stadt shows all the elements of claimed invention in figs. 1 and 2. It is an apparatus, comprising: a phase change memory [9, 10] including a phase change storage element [9, (5, 7, 8)] and a phase change threshold switch [10, (2, 4, 5)]; a conductive line [2] coupled to said phase change storage element [9] and said phase change threshold switch [10]; and a via (an area where layer [4] extends through the silicon dioxide layer [3]) to said conductive line [2].

In regards to claim 27, Technische Hochschule Karl-Marx-Stadt further discloses a barrier layer [6] between the threshold switch [10, (a portion of layer [5] under layer [6], 2, 4)] and the storage element [9, (a portion of layer [5] not under layer [6], 7, 8)].

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 3-7, 11-13, 15, 21, 23, 24, 26, 27 and 29 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Parkinson et al.

In regards to claim 1, Parkinson et al. show all the elements of the claimed invention in figs. 4-12. It is a method, comprising: forming a phase change memory [500](the devices in the middle and right side of fig. 12) including a phase change storage element [130] and a phase change threshold switch [120]; and forming a damascene via ([340] formed under the memory [500] on the left of fig. 12) (the via [340] is considered as a damascene via because it is planarized by the chemical mechanical polishing techniques) (col. 13, lines 36-45) to a conductive line [270] in the periphery of said phase change memory.

In regards to claim 3, Parkinson et al. show forming said switch [120] over said element [130].

In regards to claim 4, Parkinson et al. show forming, in said memory, a pore (the area occupied by [340]) over a substrate [240], said pore having a dimension smaller than the feature size possible with lithographic techniques (col. 13, lines 11-15).

In regards to claim 5, Parkinson et al. show forming said pore by forming an aperture [425] through an insulator [410] and forming a sidewall spacer [420] in said aperture.

In regards to claim 6, Parkinson et al. show forming a lower electrode [340] of said phase change storage element in said pore.

In regards to claim 7, Parkinson et al. show forming a barrier layer [370] between said threshold switch [120] and said storage element [130].

In regards to claim 11, Parkinson et al. show forming said phase change memory includes forming a memory array (the two memory cells [500] in the middle and right side of fig. 12) including a plurality of memory cells as a plurality of integrated islands [500] spaced from one another.

In regards to claim 12, Parkinson et al. show filling the regions surrounding said islands [500] with an insulator [510, 520].

In regards to claim 13, Parkinson et al. show forming said insulator [510, 520] to a height over the upper extent of said islands (fig. 11).

In regards to claim 15, Parkinson et al. further disclose forming a vertical groove (the area occupied by [340] on the right side of fig. 12) in said memory array and a vertical groove (the area occupied by [340] on the left side of fig. 12) in a periphery.

In regards to claim 21, Parkinson et al. show all the elements of the claimed invention in figs. 4-12. It is an apparatus, comprising: a phase change memory [500] (the device in the right side of fig. 12) including a phase change storage element [130] and a phase change threshold switch [120]; a conductive line [270] coupled to said phase change storage element [130] and said phase change threshold switch [120]; and a via ([340] formed under the memory [100] in the middle of fig. 12) to said conductive line.

In regards to claim 23, Parkinson et al. show said switch [120] is formed over said element [130].

In regards to claim 24, Parkinson et al. show said memory includes a substrate [240], a pore (the area occupied by [340]) over a substrate [240], said pore having a

dimension smaller than the feature size possible with lithographic techniques (col. 13, lines 11-15).

In regards to claim 26, Parkinson et al. show an electrode [340] for said phase change storage element [130] in said pore.

In regards to claim 27, Parkinson et al. show a barrier layer [370] between said threshold switch [120] and said storage element [130].

In regards to claim 29, Parkinson et al. show said memory includes an insulator [280] and said via ([340] formed under the memory [500] in the middle of fig. 12) includes a metal (TaN) line extending through said insulator [280].

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parkinson et al.

In regards to claim 8, Parkinson et al. show forming an upper electrode [380] over said phase change storage element [130].

Parkinson et al. differ from the claimed invention by not showing said upper electrode having a vertical extent at least twice its horizontal extent.

It would have been obvious for the upper electrode having a vertical extent at least twice its horizontal extent because it depends on the density of the memory cells in the memory.

In regards to claim 28, Parkinson et al. show an upper electrode [380] over said phase change storage element [130].

Parkinson et al. differ from the claimed invention by not showing said upper electrode having a vertical extent at least twice its horizontal extent.

It would have been obvious for the upper electrode having a vertical extent at least twice its horizontal extent because it depends on the density of the memory cells in the memory.

8. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Applicant's arguments filed 11/9/05 have been fully considered but they are not persuasive.

It is urged, in page 6 of the remarks, that the electrode could be the item 62 in fig. 16. However, there is no sidewall spacer in fig. 16. Therefore, claim 9 is vague and indefinite.

It is urged, in page 6 of the remarks, that the Applicant has provided a copy of translation in the Response. However, the examiner never received the translation of the German patent. It is also urged that item 4 is the supposed phase change layer of the asserted phase change threshold switch. Thus, the item 4 cannot possibly constitute a via, a damascene via, or a via to a conductive line in the periphery of the phase change memory since, it is not a via, it is not a damascene via, it is not a via to a conductive line, and it is not in the periphery of the phase change memory. However, a

portion of layer [4] which extends through the silicon dioxide layer [3] to said conductive line [2] is also considered as a via. Since claim 21 never discloses a damascene via or a via to a conductive line in the periphery of the phase change memory, it is not necessary for the prior art to disclose a damascene via or a via to a conductive line in the periphery of the phase change memory.

It is urged, in page 6 of the remarks, that layer 6 is an insulating layer, which is part of the memory element 9. In addition, there is no barrier layer between the memory element 9 and the decoupling element 10. Since layer [6] is an insulating layer, it is not considered as a part of the of the element [9]. Therefore, layer [6] is formed between the memory element [9] and the decoupling element [10].

It is urged, in page 7 of the remarks, that the asserted damascene via 340 is not a via in the periphery. The term "periphery" is a term of art and it means outside the memory array. However, the via [340] is still considered as a via in the periphery because the term "periphery" may also means a side portion of the memory array.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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January 20, 2006

Steven Loke
Primary Examiner